# Tutorial

# Xilinx ISE Simulator

## <Release Version: 10.1i>

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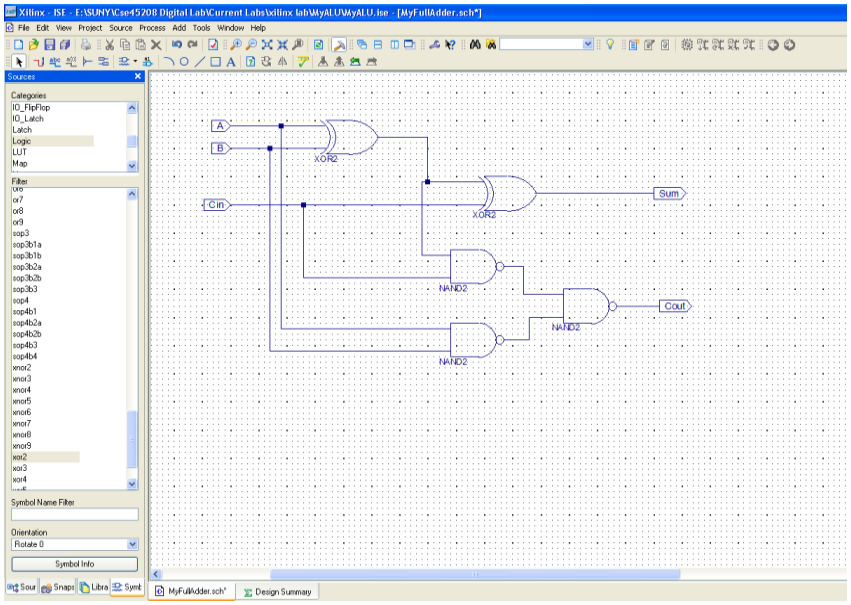
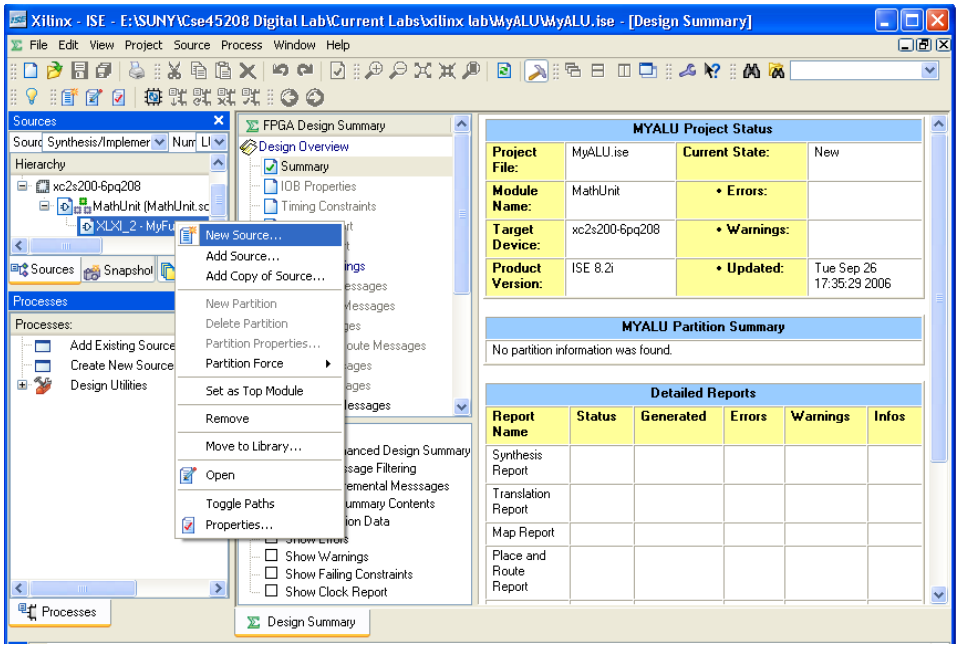
You will next test the full adder circuit that you built in the last tutorial via the ModelSIM simulation tool so that you can be sure that it functions per specification. Now lets look at our full adder.

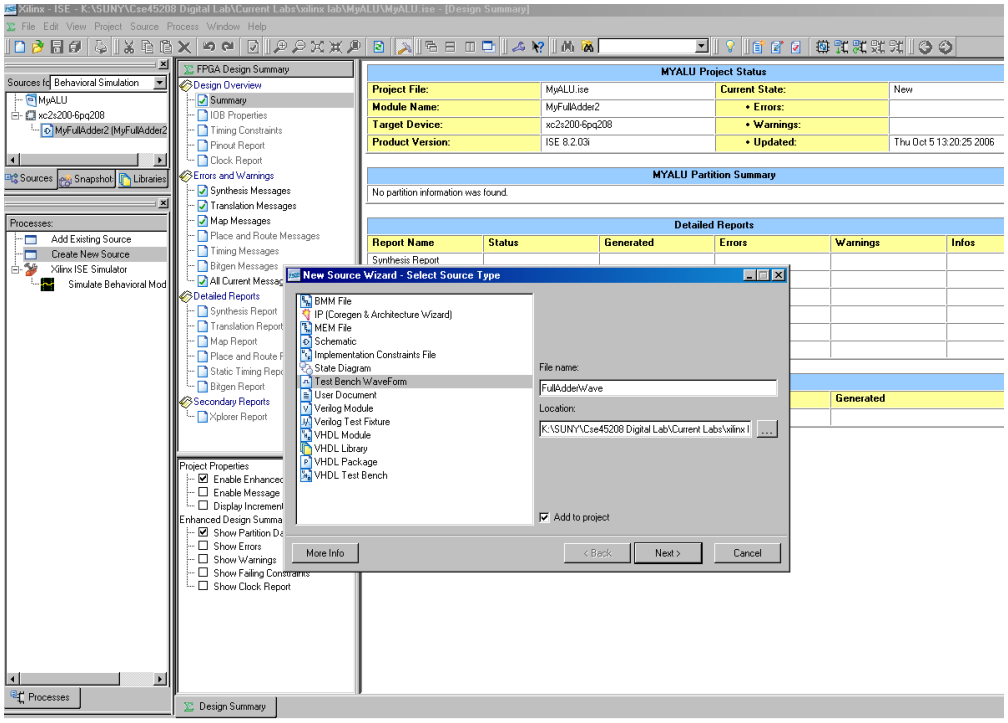



The full adder has three inputs (A, B, Cin) and two outputs (S, Cout). If you have not yet saved your schematic yet, do so and close the Schematic Editor.

Next, go back to the Project Navigator. Highlight the source that you want to simulate. In this case we want to simulate the circuit named myfulladder. Then right click on the source myfulladder and select New Source.

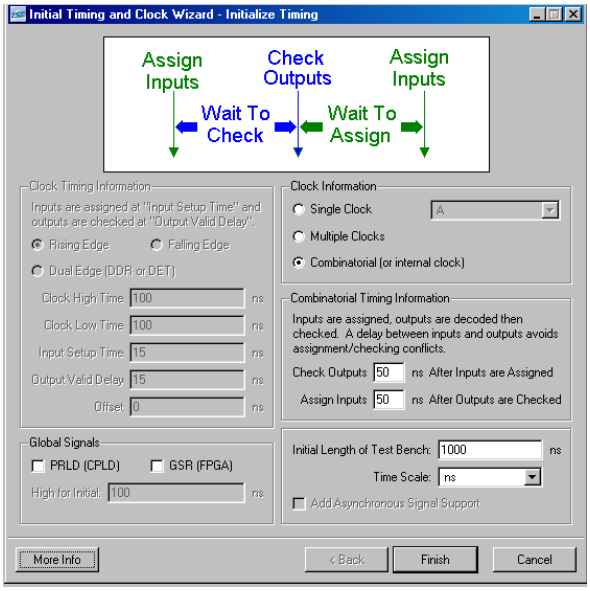



This will open a dialog box. Select “Test Bench Waveform” as the type of design entry and pick a name for your file.




Click Next!, Next! Then Finish!

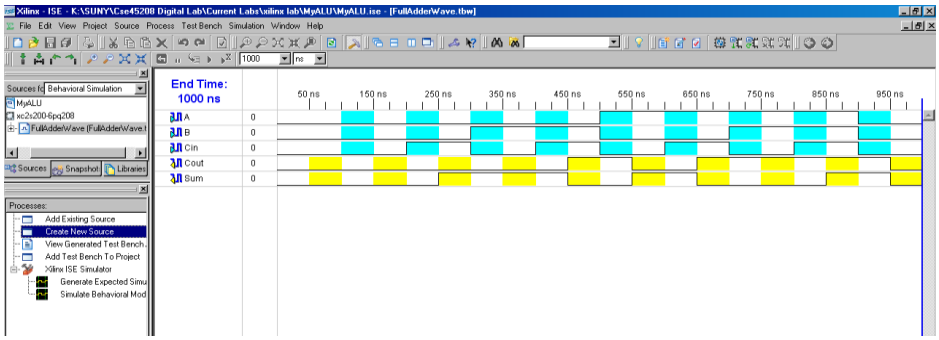
This will open up the following window:




You may change the time period of your input clock cycle, among other things. Here, the circuit is combinational. Make changes and Click Finish!!!!

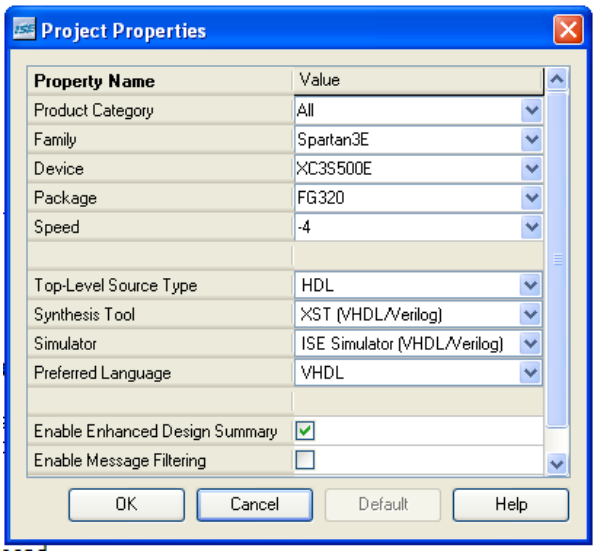
This opens the waveform window where you can select various values for the three inputs of your full adder. The input ports are marked by the blue color and the outputs by yellow. Various values (0 or 1) can be assigned to the inputs by just clicking on the blue bar corresponding to each input. Put combinations 000 through 111. On some systems, you may see the yellow bars, where you can also specify your expected value on the output by clicking on the yellow bars; If you don't see the yellow bars, don't worry and simply proceed.

The assigned values of various inputs are shown below as a waveform. A different value of input is assigned to the ports after each 100ns. This time period can be changed.



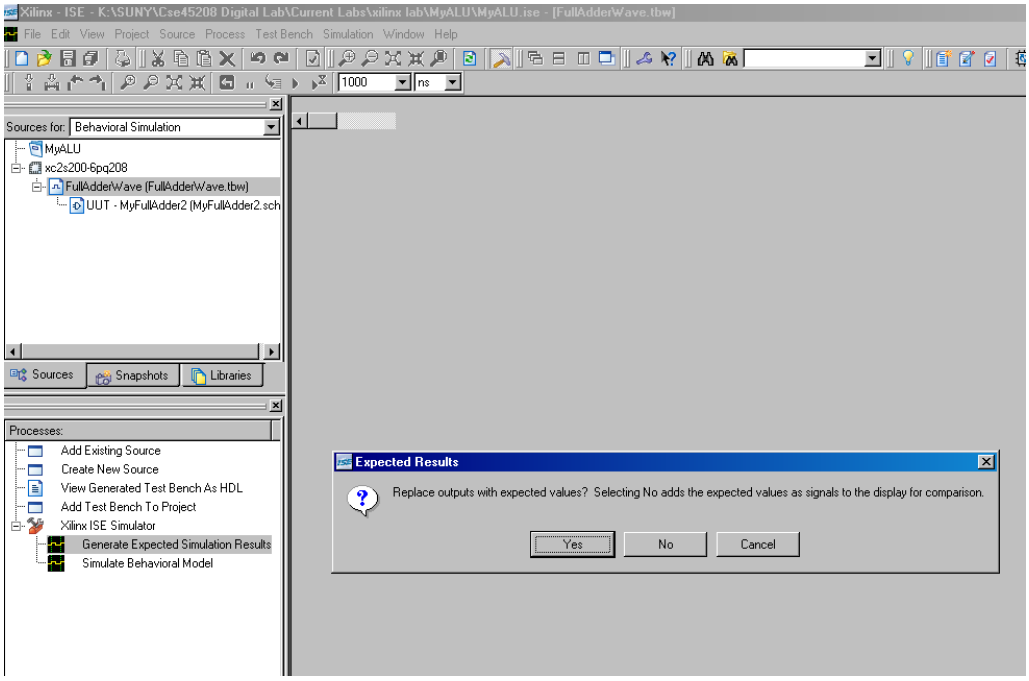

Now save the waveform.

Double click on the device XC3s500E-FG320 and make sure the selected Simulator is as ISE Simulator (VHDL/Verilog).

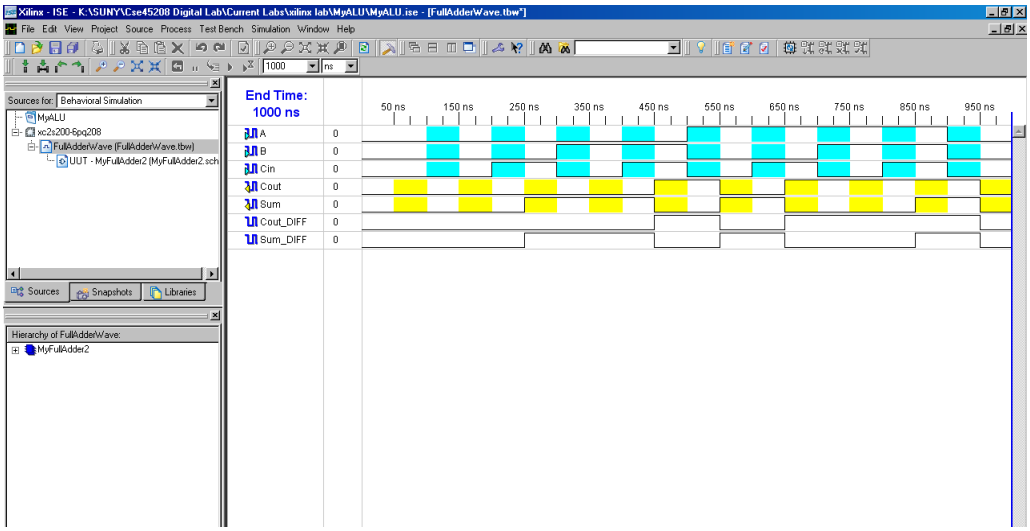



Click OK!

Click on testbench waveform file that you just created and in the Processes windows, under Xilinx ISE Simulator double click on Generate Expected Simulation Results. When prompted whether to replace the expected value choose No.

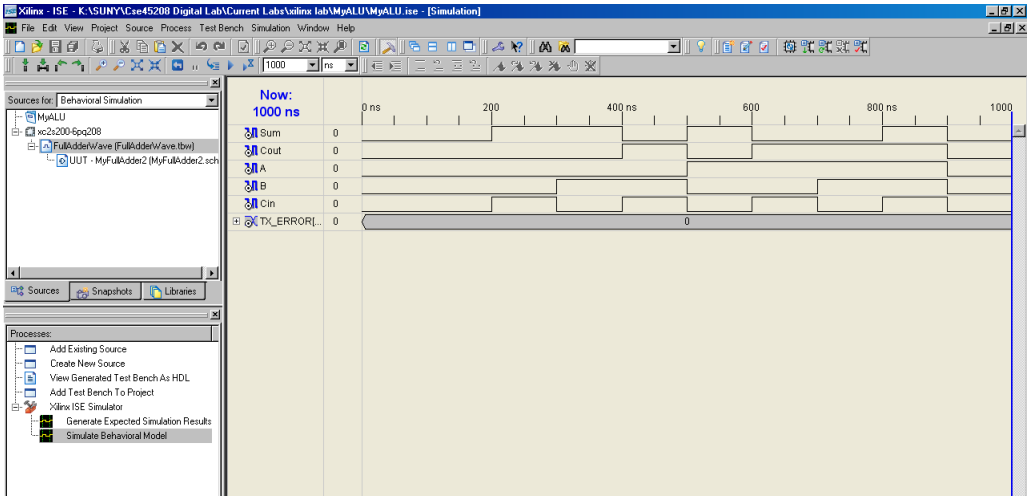


You should get the following.




Make sure the simulated results match your prediction. Once satisfied, closed the window.

In the Processes windows, under Xilinx ISE Simulator, Double Click on the "Simulate Behavioral Model".




Take a look at the Wave window. In this window You can see the waveforms of your full adder that you just simulated.